ABSTRACT OF THE DISCLOSURE

A cache memory system for use in a motion estimation system is disclosed. The system includes: a first cache memory defined in terms of a first width and a first height, and a second cache memory defined in terms of a second width and a second height, wherein said second height is less than said first height, the cache memory system being operable in one of two modes: the first mode being characterized by banks of memory from the second cache memory being concatenated vertically such that their concatenated height is at least equal to the first height, and said concatenated banks being arranged to be appended to the width of the first cache memory to form a single contiguous address space; and the second mode being characterized by banks of memory from the first and second cache being stacked vertically, and being arranged to be addressed as two separate address spaces.